REMARKS

Claims 1, 2, 4, 6, and 8 are pending in this application.

Claims 2, 4, 6, and 9-12 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,115,410 to Naruse (hereinafter "Naruse"). Claims 1, 3, 5, 7, and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Naruse in view of U.S. Patent No. 6,262,751 to Chan (hereinafter "Chan").

By the foregoing amendments, Applicant has canceled claims 3, 5, 7, and 9-12 and has amended claims 2, 4, and 6 to incorporate the subject matter of claims 3, 5, and 7 respectively; namely, to incorporate the bit reordering means into the independent claims. Claim 8 has been amended to depend from claim 6. Additional minor editorial revisions have been made to the claims to clarify the operation of the present invention and to further distinguish the present invention over the cited references. Two minor editorial revisions were made to the specification to correct typographical errors.

Naruse relates to a Walsh code generator, including a binary counter, a parallel generation controller, and a Walsh code parallel generator. The counter controls the position of an output bit in the Walsh code. The parallel generation controller controls an upper portion of the Walsh code, and the Walsh code parallel generator controls a lower portion of the Walsh code. The parallel generator

controller includes a plurality of AND gates, the outputs of the AND gates being connected to a plurality of XOR gates. (See Figures 3-4 and column 5, lines 26-67.)

Chan relates to a display controller for rotating an image to be shown on a computer display, particularly between "landscape" and "portrait" display modes. As shown in Figure 10, the display controller includes three switch stages (94, 96, 98), and each switch stage includes four switch circuits (94a-94d) (column 6, lines 53-57 and column 7, lines 1-15). As noted at column 7, lines 5-8:

> the upper half of the switch circuits in a given stage receives the odd-numbered bits in descending order, while the lower ones receive the even-numbered bits in descending order.

In the Office Action, the Examiner states that Chan discloses bit ordering means, for selectively reordering the bits of each binary number from least significant bit to most significant bit (page 7, paragraph 15 of the Office Action). As described above, Chan discloses grouping the odd-numbered bits and the even-numbered bits together in descending order. This is clearly not the same as reordering bits from least significant to most significant (or from most significant to least significant), as is recited in claims 1, 2, 4, and 6 of the present application.

Therefore, the present application is distinguishable over Naruse and Chan. It is respectfully submitted that the amendments and remarks made herein place pending claims 1, 2, 4, 6, and 8 in condition for allowance. Accordingly, entry of this

amendment as well as reconsideration and allowance of pending claims 1, 2, 4, 6, and 8 are respectfully requested.

If the Examiner does not believe that the claims are in condition for allowance, the Examiner is respectfully requested to contact the undersigned at 215-568-6400.

Respectfully submitted,

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